





EH49 20 ET

Series — RoHS Compliant (Pb-free) 1.8V 4 Pad 2.5mm x 3.2mm Ceramic SMD LVCMOS Oscillator

Frequency Tolerance/Stability — ±20ppm Maximum

Operating Temperature Range --40°C to +85°C

TS -27.000M

Nominal Frequency 27.000MHz

Pin 1 Connection
Tri-State (High Impedance)

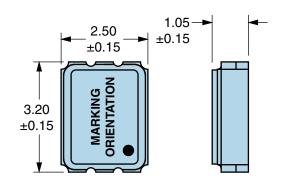
- Duty Cycle 50 ±10(%)

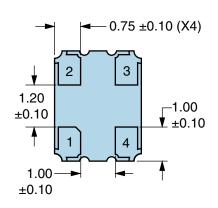
Operating Temperature Range, Supply Voltage Change, Output Load Change, First Year Aging at 25°, 260°C Reflow, Shock, and Vibration) Aging at 25°C	ELECTRICAL SPECIFICATIONS		
Operating Temperature Range, Supply Voltage Change, Output Load Change, First Year Aging at 25°, 260°C Reflow, Shock, and Vibration) Aging at 25°C	Nominal Frequency	27.000MHz	
Operating Temperature Range -40°C to +85°C Supply Voltage 1.8Vdc ±5% Input Current 4mA Maximum (No Load) Output Voltage Logic High (Voh) 90% of Vdd Minimum (IOH = -8mA) Output Voltage Logic Low (Vol) 10% of Vdd Maximum (IOL = +8mA) Rise/Fall Time 6nSec Maximum (Measured at 20% to 80% of waveform) Duty Cycle 50 ±10(%) (Measured at 50% of waveform) Load Drive Capability 15pF Maximum Output Logic Type CMOS Pin 1 Connection Tri-State (High Impedance) Tri-State Input Voltage (Vih and Vil) 90% of Vdd Minimum or No Connect to Enable Output, 10% of Vdd Maximum to Disable Output (High Impedance) Standby Current 10µA Maximum (Pin 1 = Ground) Absolute Clock Jitter ±125pSec Maximum Start Up Time 10mSec Maximum	Frequency Tolerance/Stability	±20ppm Maximum (Inclusive of all conditions: Calibration Tolerance at 25°C, Frequency Stability over the Operating Temperature Range, Supply Voltage Change, Output Load Change, First Year Aging at 25°, 260°C Reflow, Shock, and Vibration)	
Supply Voltage Input Current 4mA Maximum (No Load) Output Voltage Logic High (Voh) 90% of Vdd Minimum (IOH = -8mA) Output Voltage Logic Low (Vol) 10% of Vdd Maximum (IOL = +8mA) Rise/Fall Time 6nSec Maximum (Measured at 20% to 80% of waveform) Duty Cycle 50 ±10(%) (Measured at 50% of waveform) Load Drive Capability 15pF Maximum Output Logic Type CMOS Pin 1 Connection Tri-State (High Impedance) Tri-State Input Voltage (Vih and Vil) 90% of Vdd Minimum or No Connect to Enable Output, 10% of Vdd Maximum to Disable Output (High Impedance) Standby Current 10µA Maximum (Pin 1 = Ground) Absolute Clock Jitter \$10mSec Maximum	Aging at 25°C	±5ppm/Year Maximum	
Input Current 4mA Maximum (No Load) Output Voltage Logic High (Voh) 90% of Vdd Minimum (IOH = -8mA) Output Voltage Logic Low (Vol) 10% of Vdd Maximum (IOL = +8mA) Rise/Fall Time 6nSec Maximum (Measured at 20% to 80% of waveform) Duty Cycle 50 ±10(%) (Measured at 50% of waveform) Load Drive Capability 15pF Maximum Output Logic Type CMOS Pin 1 Connection Tri-State (High Impedance) Tri-State Input Voltage (Vih and Vil) 90% of Vdd Minimum or No Connect to Enable Output, 10% of Vdd Maximum to Disable Output (High Impedance) Standby Current 10μA Maximum (Pin 1 = Ground) Absolute Clock Jitter ±125pSec Maximum 10mSec Maximum	Operating Temperature Range	-40°C to +85°C	
Output Voltage Logic High (Voh) Output Voltage Logic Low (Vol) 10% of Vdd Minimum (IOH = -8mA) Rise/Fall Time 6nSec Maximum (Measured at 20% to 80% of waveform) Duty Cycle 50 ±10(%) (Measured at 50% of waveform) Load Drive Capability 15pF Maximum Output Logic Type CMOS Pin 1 Connection Tri-State (High Impedance) Tri-State Input Voltage (Vih and Vil) 90% of Vdd Minimum or No Connect to Enable Output, 10% of Vdd Maximum to Disable Output (High Impedance) Standby Current 10µA Maximum (Pin 1 = Ground) Absolute Clock Jitter ±125pSec Maximum 10mSec Maximum	Supply Voltage	1.8Vdc ±5%	
Output Voltage Logic Low (Vol) 10% of Vdd Maximum (IOL = +8mA) Rise/Fall Time 6nSec Maximum (Measured at 20% to 80% of waveform) Duty Cycle 50 ±10(%) (Measured at 50% of waveform) Load Drive Capability 15pF Maximum Output Logic Type CMOS Pin 1 Connection Tri-State (High Impedance) Tri-State Input Voltage (Vih and Vil) 90% of Vdd Minimum or No Connect to Enable Output, 10% of Vdd Maximum to Disable Output (High Impedance) Standby Current 10μA Maximum (Pin 1 = Ground) Absolute Clock Jitter ±125pSec Maximum Start Up Time 10mSec Maximum	Input Current	4mA Maximum (No Load)	
Rise/Fall Time 6nSec Maximum (Measured at 20% to 80% of waveform) Duty Cycle 50 ±10(%) (Measured at 50% of waveform) Load Drive Capability 15pF Maximum Output Logic Type CMOS Pin 1 Connection Tri-State (High Impedance) Tri-State Input Voltage (Vih and Vil) 90% of Vdd Minimum or No Connect to Enable Output, 10% of Vdd Maximum to Disable Output (High Impedance) Standby Current 10µA Maximum (Pin 1 = Ground) Absolute Clock Jitter ±125pSec Maximum Start Up Time 10mSec Maximum	Output Voltage Logic High (Voh)	90% of Vdd Minimum (IOH = -8mA)	
Duty Cycle 50 ±10(%) (Measured at 50% of waveform) Load Drive Capability 15pF Maximum Output Logic Type CMOS Pin 1 Connection Tri-State (High Impedance) Tri-State Input Voltage (Vih and Vil) 90% of Vdd Minimum or No Connect to Enable Output, 10% of Vdd Maximum to Disable Output (High Impedance) Standby Current 10µA Maximum (Pin 1 = Ground) Absolute Clock Jitter ±125pSec Maximum Start Up Time 10mSec Maximum	Output Voltage Logic Low (Vol)	10% of Vdd Maximum (IOL = +8mA)	
Load Drive Capability 15pF Maximum Output Logic Type CMOS Pin 1 Connection Tri-State (High Impedance) Tri-State Input Voltage (Vih and Vil) 90% of Vdd Minimum or No Connect to Enable Output, 10% of Vdd Maximum to Disable Output (High Impedance) Standby Current 10µA Maximum (Pin 1 = Ground) Absolute Clock Jitter ±125pSec Maximum Start Up Time 10mSec Maximum	Rise/Fall Time	6nSec Maximum (Measured at 20% to 80% of waveform)	
Output Logic Type CMOS Pin 1 Connection Tri-State (High Impedance) Tri-State Input Voltage (Vih and Vil) 90% of Vdd Minimum or No Connect to Enable Output, 10% of Vdd Maximum to Disable Output (High Impedance) Standby Current 10µA Maximum (Pin 1 = Ground) Absolute Clock Jitter ±125pSec Maximum Start Up Time 10mSec Maximum	Duty Cycle	50 ±10(%) (Measured at 50% of waveform)	
Pin 1 Connection Tri-State (High Impedance) Tri-State Input Voltage (Vih and Vil) 90% of Vdd Minimum or No Connect to Enable Output, 10% of Vdd Maximum to Disable Output (High Impedance) Standby Current 10µA Maximum (Pin 1 = Ground) Absolute Clock Jitter ±125pSec Maximum Start Up Time 10mSec Maximum	Load Drive Capability	15pF Maximum	
Tri-State Input Voltage (Vih and Vil) 90% of Vdd Minimum or No Connect to Enable Output, 10% of Vdd Maximum to Disable Output (High Impedance) Standby Current 10μA Maximum (Pin 1 = Ground) Absolute Clock Jitter ±125pSec Maximum Start Up Time 10mSec Maximum	Output Logic Type	CMOS	
Impedance) Standby Current 10μA Maximum (Pin 1 = Ground) Absolute Clock Jitter ±125pSec Maximum Start Up Time 10mSec Maximum	Pin 1 Connection	Tri-State (High Impedance)	
Absolute Clock Jitter ±125pSec Maximum Start Up Time 10mSec Maximum	Tri-State Input Voltage (Vih and Vil)	, ,	
Start Up Time 10mSec Maximum	Standby Current	10μA Maximum (Pin 1 = Ground)	
	Absolute Clock Jitter	±125pSec Maximum	
Storage Temperature Range -55°C to +125°C	Start Up Time	10mSec Maximum	
	Storage Temperature Range	-55°C to +125°C	

ENVIRONMENTAL & MECHANICAL SPECIFICATIONS		
ESD Susceptibility	MIL-STD-883, Method 3015, Class 1, HBM: 1500Vdc	
Fine Leak Test	MIL-STD-883, Method 1014, Condition A	
Flammability	UL94-V0	
Gross Leak Test	MIL-STD-883, Method 1014, Condition C	
Mechanical Shock	MIL-STD-883, Method 2002, Condition B	
Moisture Resistance	MIL-STD-883, Method 1004	
Moisture Sensitivity	J-STD-020, MSL 1	
Resistance to Soldering Heat	MIL-STD-202, Method 210, Condition K	
Resistance to Solvents	MIL-STD-202, Method 215	
Solderability	MIL-STD-883, Method 2003	
Temperature Cycling	MIL-STD-883, Method 1010, Condition B	
Vibration	MIL-STD-883, Method 2007, Condition A	



MECHANICAL DIMENSIONS (all dimensions in millimeters)



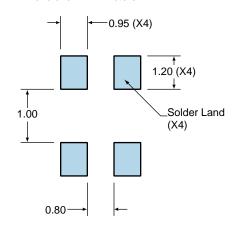


PIN	CONNECTION
1	Tri-State
2	Case Ground
3	Output
4	Supply Voltage

LINE	MARKING
1	EPO
_	XXXXX XXXXX=Ecliptek Manufacturing Identifier

Suggested Solder Pad Layout

All Dimensions in Millimeters



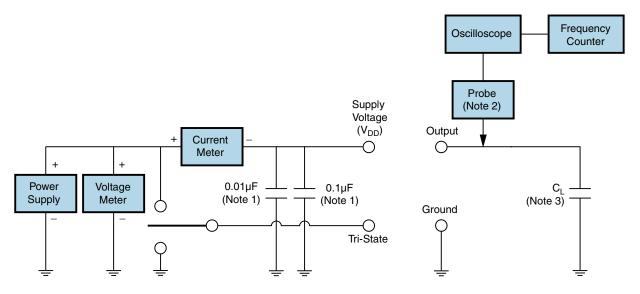
All Tolerances are ±0.1



OUTPUT WAVEFORM & TIMING DIAGRAM



Test Circuit for CMOS Output



- Note 1: An external 0.01µF ceramic bypass capacitor in parallel with a 0.1µF high frequency ceramic bypass capacitor close (less than 2mm) to the package ground and supply voltage pin is required.
- Note 2: A low capacitance (<12pF), 10X attenuation factor, high impedance (>10Mohms), and high bandwidth (>300MHz) passive probe is recommended.
- Note 3: Capacitance value C₁ includes sum of all probe and fixture capacitance.



Recommended Solder Reflow Methods



High Temperature Infrared/Convection

T _s MAX to T _∟ (Ramp-up Rate)	3°C/second Maximum
Preheat	
- Temperature Minimum (Ts MIN)	150°C
- Temperature Typical (T _s TYP)	175°C
- Temperature Maximum (T _s MAX)	200°C
- Time (t _s MIN)	60 - 180 Seconds
Ramp-up Rate (T _L to T _P)	3°C/second Maximum
Time Maintained Above:	
- Temperature (T∟)	217°C
- Time (t∟)	60 - 150 Seconds
Peak Temperature (T _P)	260°C Maximum for 10 Seconds Maximum
Target Peak Temperature (T _P Target)	250°C +0/-5°C
Time within 5°C of actual peak (tp)	20 - 40 seconds
Ramp-down Rate	6°C/second Maximum
Time 25°C to Peak Temperature (t)	8 minutes Maximum
Moisture Sensitivity Level	Level 1



Recommended Solder Reflow Methods



Low Temperature Infrared/Convection 240°C

T _S MAX to T _L (Ramp-up Rate)	5°C/second Maximum
Preheat	
- Temperature Minimum (T _s MIN)	N/A
- Temperature Typical (T _S TYP)	150°C
- Temperature Maximum (T _s MAX)	N/A
- Time (t _s MIN)	60 - 120 Seconds
Ramp-up Rate (T _L to T _P)	5°C/second Maximum
Time Maintained Above:	
- Temperature (T∟)	150°C
- Time (t∟)	200 Seconds Maximum
Peak Temperature (T _P)	240°C Maximum
Target Peak Temperature (T _P Target)	240°C Maximum 1 Time / 230°C Maximum 2 Times
Time within 5°C of actual peak (tp)	10 seconds Maximum 2 Times / 80 seconds Maximum 1 Time
Ramp-down Rate	5°C/second Maximum
Time 25°C to Peak Temperature (t)	N/A
Moisture Sensitivity Level	Level 1

Low Temperature Manual Soldering

185°C Maximum for 10 seconds Maximum, 2 times Maximum.

High Temperature Manual Soldering

260°C Maximum for 5 seconds Maximum, 2 times Maximum.